200W Push-Pull & 110W Single-Ended High Performance RF-LDMOS Transistors for WCDMA Basestation Applications

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Abstract — **The performance of a 200W push-pull device and a 110W single-ended device, both using state-of-the-art silicon RF-LDMOS die technology, is described. In the 2.1GHz band with a two-carrier WCDMA signal applied and a supply voltage of 28V, –37dBc IM3 and 25-26% drain efficiency is achieved at 38W and 19W respectively for the two devices. This combination of linear power and efficiency make these devices ideally suited for power amplifier designs in basestation transceiver systems.**

I. Introduction

For several years silicon LDMOS has been the dominant basestation amplifier technology. Offering a combination of linearity, efficiency, cost, and reliability currently unparalleled in the field [1]-[3], RF-LDMOS has emerged as the driving device technology for the basestation industry. The work described in this paper is believed by the authors to be a new benchmark in RF-LDMOS performance.

The devices discussed are a 200W (P1dB) push-pull design using four die with 80mm of gate width each (Fig.1) and a 110W (P1dB) single-ended design which uses two 80mm die (Fig.2). Both designs employ internal matching at the input and output to allow for easier matching across the 2110-2170 MHz band. Higher power parts are available, but these two parts are currently in the highest demand and will hence be the focus of this paper.

	Freq.	Zin(Ω)	Zout(Ω)
200W PP	2110MHz	5.39-j13.89	3.69-j10.51
	2140MHz	5.66-j13.99	3.81-j10.66
	2170MHz	5.53-j14.51	3.79-j11.05
110W SE	2100MHz	3.4-j5.1	2.4-j2.0
	2120MHz	3.2-j5.4	2.2-j2.1
	2160MHz	3.0-j4.4	2.1-j1.9
	2200MHz	3.0-j4.0	1.8-j1.6

Table. 1. Input/Output Impedances Across WCDMA Band

II. Device Structure & Design

RF-LDMOS is a modified n-channel MOSFET specifically designed for power amplifier applications. Using a laterally diffused p-type implant to create the channel of the transistor along with a carefully engineered LDD region, high supply voltages can be applied without premature punchthrough or breakdown occurring during large signal swings. These parts are fabricated using

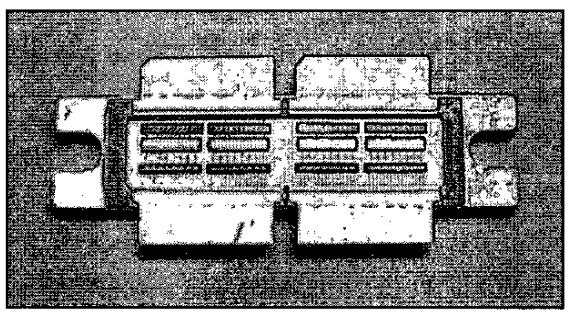

Fig. 1. 200W push-pull device with four 80mm die and input/output internal matching.

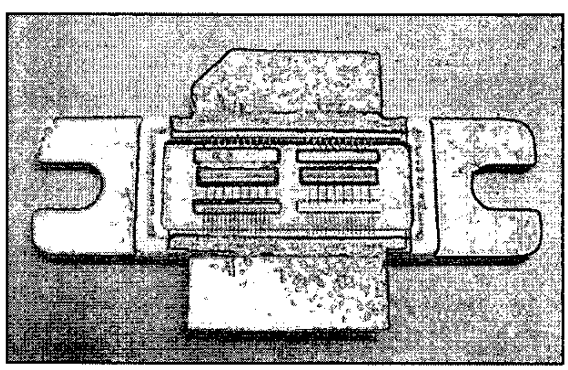

Fig. 2. 110W single-ended device with two 80mm die and input/output internal matching.

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Motorola's 5th generation RF-LDMOS technology, HV5, and yields a BV_{DSS} in excess of 68V. A p+ sinker implant is used to provide a low resistance low inductance path to ground via the p+ substrate. HV5 uses an improved grounded Faraday shield to prevent excessive feedback from occurring by reducing C_{gd}. For thermal management reasons the die is thinned to 4 mils and eutectically attached to the CuW packages pictured in Figs. 1 & 2. The flanges for these packages are 65mils and 40mils respectively.

The internal matching for both designs consists of a single stage network for both input and output matching. A low pass T-network is used for the input matching and a high pass shunt-L network for the output matching. The resultant impedances achieved with these internal matching designs are shown in Table 1.

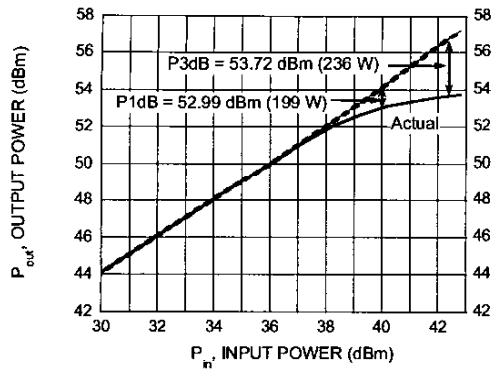

Fig. 3. Pulsed CW Output Power vs. Input Power for the 200W push-pull design. [VDC=28V, IDQ=1600mA, pulsed CW 8µsec(on)/1msec(off), center frequency = 2140MHz]

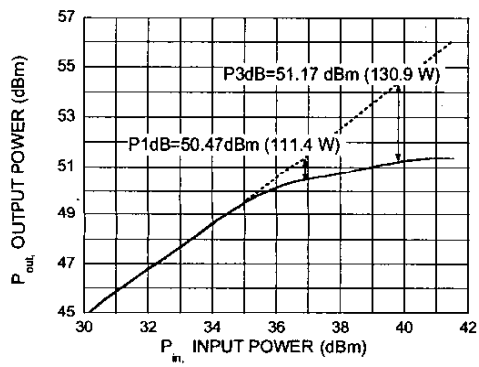

Fig. 4. Pulsed CW Output Power vs. Input Power for the 110W push-pull design. [VDC=28V, IDQ=850mA, pulsed CW 8µsec(on)/1msec(off), center frequency = 2140MHz]

III. PERFORMANCE

Figs. 3 & 4 illustrate the drive-up performance, under pulsed CW conditions, at 2.14GHz, of the two devices. Despite the low average power requirements of WCDMA applications, high peak-to-average ratios dictate that the parts have excellent output compression capabilities. Using a pulsed CW signal [8µsec(on)/1msec(off)], the ability of the devices to handle the signal peaks can be estimated. The push-pull part delivers 199W (P1dB) and the single-ended delivers 111W (P1dB). The P3dB compression powers are 236W and 131W respectively. Power per unit of gate periphery based on the P1dB numbers is roughly 650mW/mm.

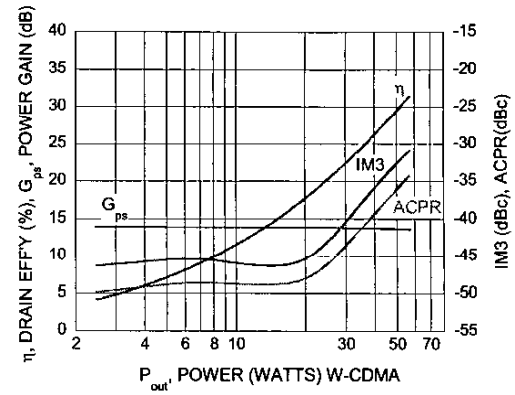

Fig. 5. Two-carrier WCDMA ACPR, IM3, Power Gain, and Drain Efficiency vs. Output Power for the 200W push-pull design. [VDC=28V, IDQ=1600mA, 10MHz carrier spacing, 3.84MHz channel bandwidth, peak/avg=8.5dB @ 0.01% probability (CCDF)]

A two-carrier WCDMA signal with an 8.5dB peak to average ratio at 0.01% probability (CCDF) per carrier was used to quantify the performance of the devices under a digital modulation scheme. A 10MHz carrier spacing was used (f1=2135MHz, f2=2145MHz) with a channel bandwidth of 3.84MHz. The drive-up curves plotted in Figs. 5 & 6 clearly show the excellent linear power capability of these parts. The push-pull part achieves 38W average output power at –37dBc with 25% drain efficiency and 14dB of gain. The single-ended design delivers 19W at –37dBc with 26% drain efficiency and 14.5dB of gain In addition it should be noted that under

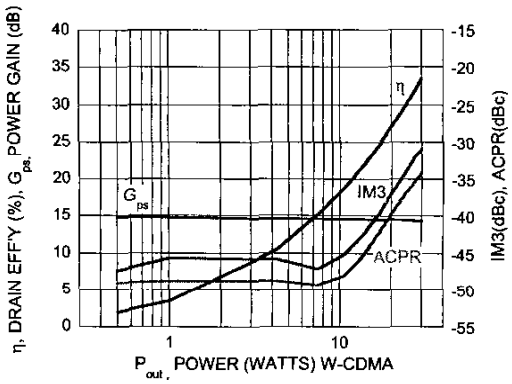

Fig. 6. Two-carrier WCDMA ACPR, IM3, Power Gain, and Drain Efficiency vs. Output Power for the 110W single-ended design. [VDC=28V, IDQ=850mA, 10MHz carrier spacing, 3.84MHz channel bandwidth, peak/avg=8.5dB @ 0.01% probability (CCDF)]

backoff conditions the IM3 descends below –45dBc – a level of backoff linearity not commonly observed on GaAs transistors.

As an example of how the designs perform across the bandwidth of 2110MHz to 2170MHz, Fig. 7 is included which shows the broadband performance of the 200W

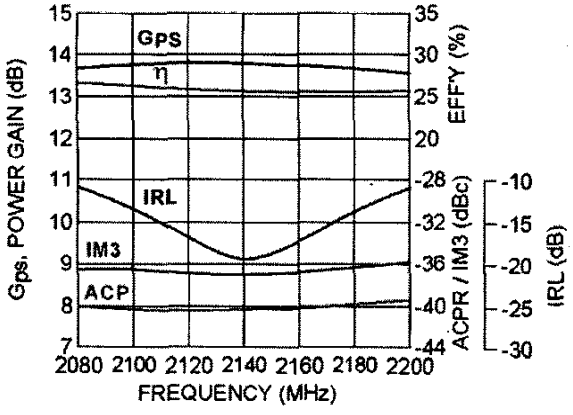

Fig. 7. Two-carrier WCDMA Broadband Performance for the 200W push-pull design. [VDC=28V, Pout(avg)=38W, IDQ=1600mA, 10MHz carrier spacing, 3.84MHz channel bandwidth, peak/avg=8.5dB @ 0.01% probability (CCDF)]

push-pull device. It is shown that a gain flatness of 0.1 dB is achievable over the entire bandwidth, with excellent efficiency and linearity. This curve also shows that efficiency improvements over previous generations are in fact true across the entire WCDMA frequency band.

III. Reliability

An important tradeoff that needs to be considered when engineering an LDMOS part for superior RF performance is reliability, specifically hot carrier injection (HCI). Due to the large supply voltages applied on the drain of the device, large electric fields are present which can lend excessive energy to the charge carriers in the channel of the transistor. Under these conditions, some carriers will be injected into the gate oxide and serve to increase the threshold voltage of the device over time. This shift in VT will slowly change the quiescent drain bias current (IDQ) thus altering the load line and degrading the RF

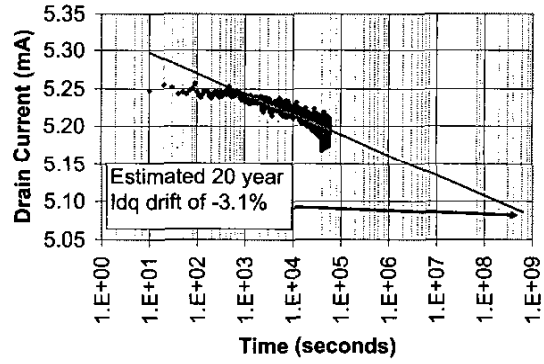

Fig. 8. IDQ vs. Time Under HCI DC Stress Conditions. [1.2mm device, VD=28V, VG=3.73V]

performance.

As a measure of quantifying this HCI effect, testing is done both at the wafer and package part level to get an estimate of the percentage impact on IDQ. For the HV5 technology discussed in this paper, Fig. 8 shows a typical HCI response. The device under test is a 1.2mm version of the 80mm die used in the push-pull and single-ended designs. A drain voltage of 28V was applied to the device and a gate voltage of 3.73V was used to set an IDQ of roughly 5.0mA/mm. The part was then stressed with these DC biases for approximately 16 hours. Using a logarithmic extrapolation out to 20 years an estimate of the percent IDQ drift is obtained. The resultant 3.1% illustrates the extremely high level of HCI reliability that has been designed into the transistor.

IV. Conclusion

Performance and reliability data for a 110W single-ended and a 200W push-pull devices fabricated using

Motorola's 5th generation HV5 RF-LDMOS platform have been presented. In the 2.1GHz band with a two-carrier WCDMA signal applied and a supply voltage of 28V, the push-pull part provides 38W and 25% efficiency at -37dBc IM3, while the single-ended device provides 19W and 26% efficiency at -37dBc IM3. These high performance levels were achieved without compromising the HCI performance (estimated 3.1% quiescent current drift in 20 years). These devices, along with other devices in the HV5 platform, represent the state-of-the-art in cellular infrastructure RF power amplifier device technology.

REFERENCES

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